

CXA3815N

Description

Audio IC for LCD-TV's

Features

- ◆ Operating voltage $V_{CC} = 3.0$ to $3.6V$
- ◆ Differential input
- ◆ Output decoupling capacitor less
- ◆ Gain switching function (6dB/12dB)
- ◆ Mute function

Structure

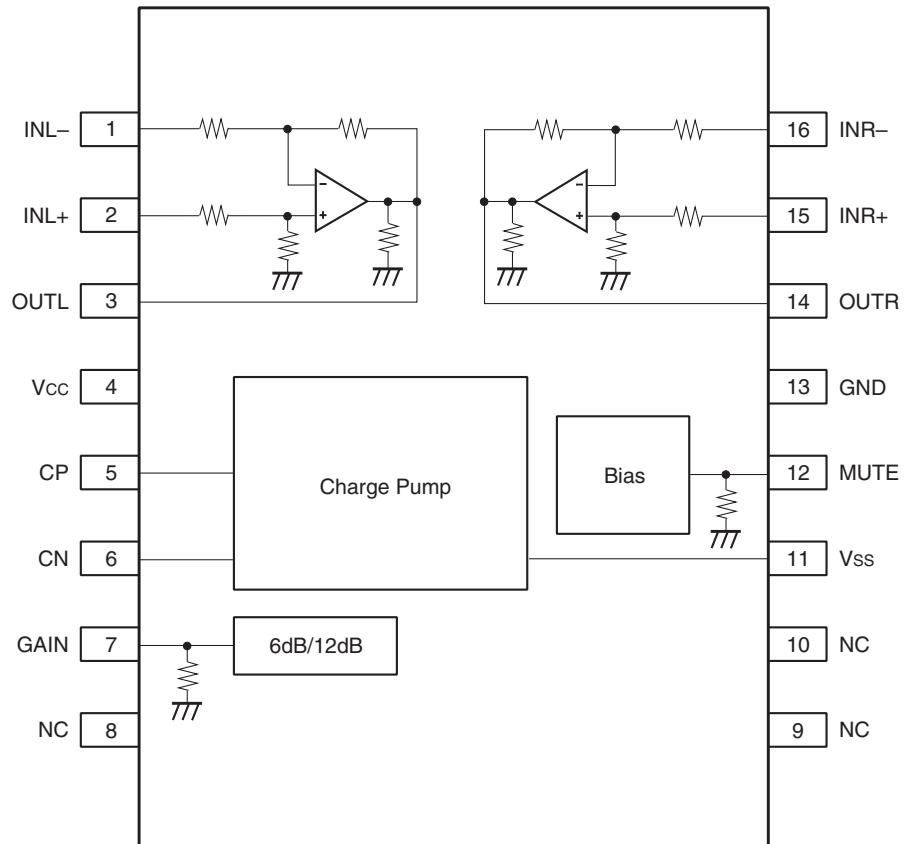
BiCMOS monolithic IC

Package

SSOP-16P

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Block Diagram



Pin Description

Pin No.	Symbol	I/O	Pin voltage [V]		Equivalent circuit	Description
			DC	AC		
1	INL-	I	0	—		HP AMP_L input (-)
16	INR-	I	0	—		HP AMP_R input (-)
2	INL+	I	0	—		HP AMP_L input (+)
15	INR+	I	0	—		HP AMP_R input (+)
3	OUTL	O	0	—		HP AMP_L output
14	OUTR	O	0	—		HP AMP_R output

Pin No.	Symbol	I/O	Pin voltage [V]		Equivalent circuit	Description
			DC	AC		
5	CP	I/O	—	3.3		CP capacitance connection
6	CN	I/O	—	-3.3		CP capacitance connection
11	Vss	I/O	-3.26	—		Vss
7	GAIN	I	0	—		Gain switching
12	MUTE	I	0	—		Mute switching
4	Vcc	I/O	—	—		Vcc
13	GND	I/O	—	—		GND

Electrical Characteristics

Unless otherwise specified

($V_{CC} = 3.3V$, $T_a = 25^{\circ}C$, $f_{signal} = 1kHz$, differential input, Measurement band width = 20Hz to 20kHz)

Power

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
Maximum rating	V_{max}		—	—	4.5	V
Operating temperature	T_a		-25	—	+85	$^{\circ}C$

Amplifier Block

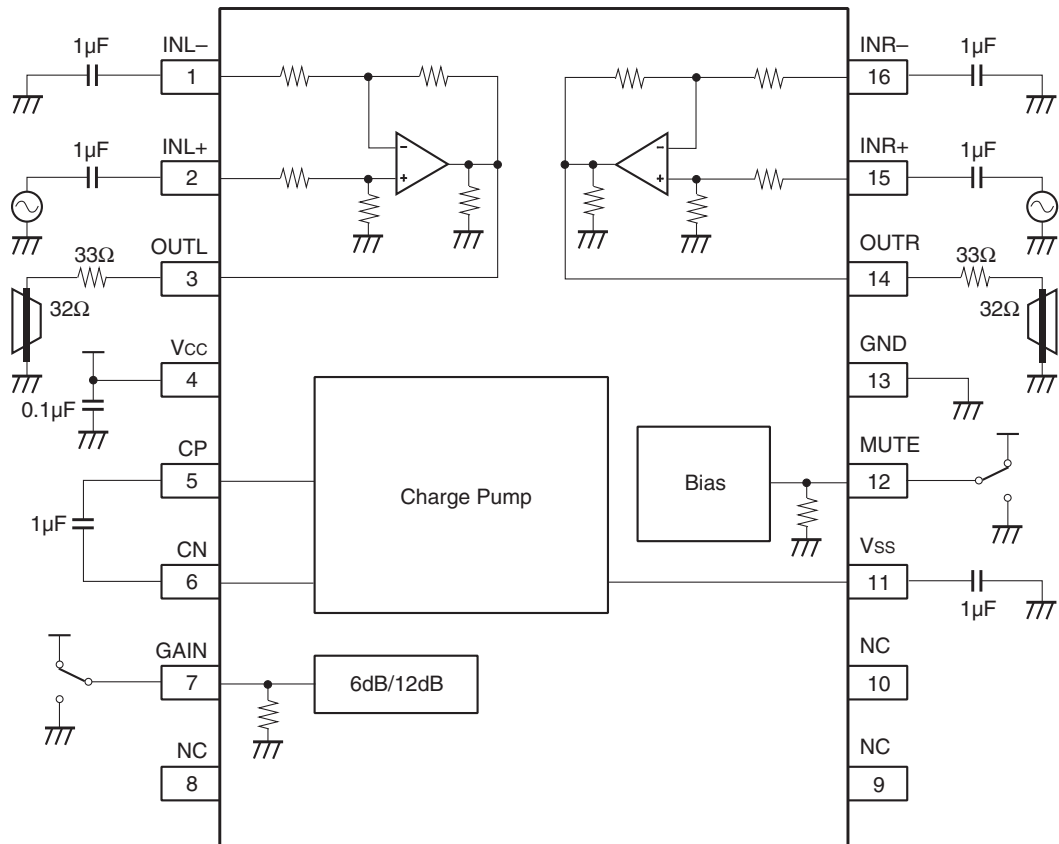
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input impedance	R_{in}		96	120	144	$k\Omega$
Gain1	G_{v1}	GAIN Low, 0.1Vrms input	5.5	6	6.5	dB
Gain2	G_{v2}	GAIN High, 0.1Vrms input	11.5	12	12.5	dB
Total harmonic distortion 1	THD1	$R_L = 33 + 32\Omega$ GAIN Low, 0.1Vrms input	—	0.01	0.1	%
Total harmonic distortion 2	THD2	$R_L = 33 + 32\Omega$, $P_o = 15mW$ GAIN Low	—	—	0.5	%
Total harmonic distortion 3	THD3	$R_L = 470 + 10k\Omega$, $V_o = 2.0V_{rms}$ GAIN Low	—	—	1	%
Output noise level	V_{no}	No signal input, measured at 32Ω ends	—	-100	-95	dBv
Channel separation	CS	$R_L = 33 + 32\Omega$, $P_o = 15mW$ 1kHz BPF, GAIN Low	70	80	—	dB
DC offset	V_{os}	No signal input, GAIN Low	-5	—	5	mV
Mute level	V_{mute}	$R_L = 33 + 32\Omega$, $P_o = 15mW$ GAIN Low, MUTE ON	—	-70	-60	dB

Control Block

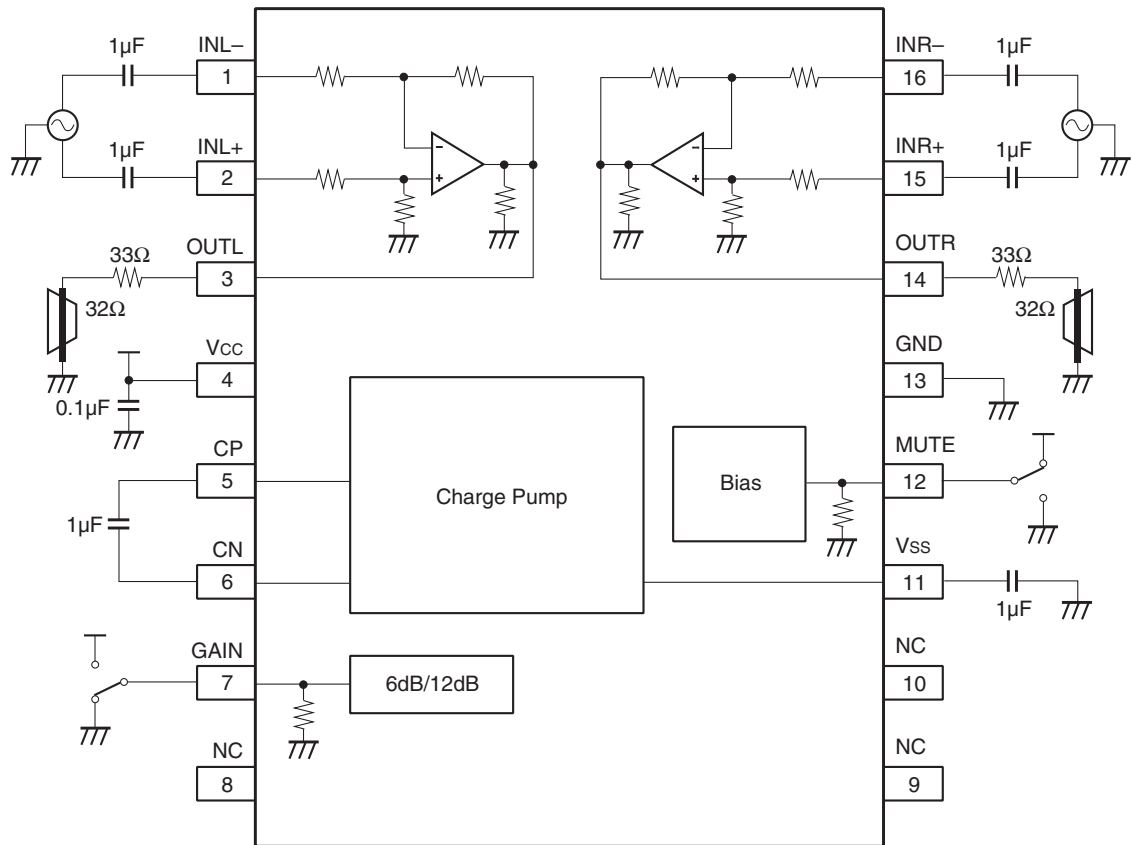
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Mute H	MuteH	Mute = OFF	$0.7V_{CC}$	—	V_{CC}	V
Mute L	MuteL	Mute = ON	0	—	0.8	V
Gain H	GainH	Gain = 12dB	$0.7V_{CC}$	—	V_{CC}	V
Gain L	GainL	Gain = 6dB	0	—	0.8	V

Application Circuit

Single Input



Differential Input





Notes On Handling

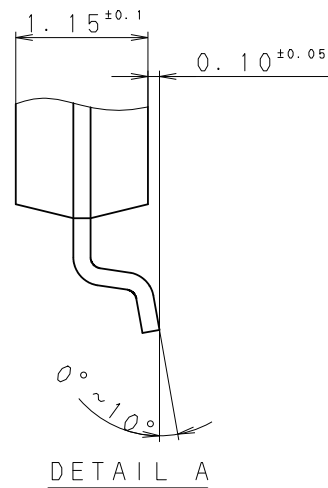
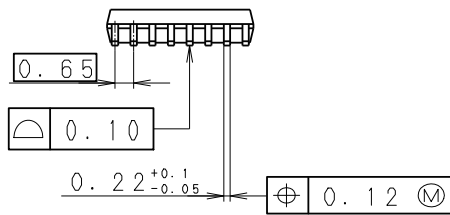
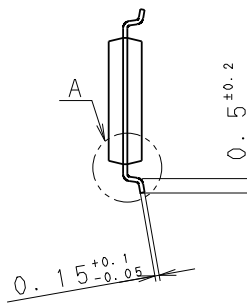
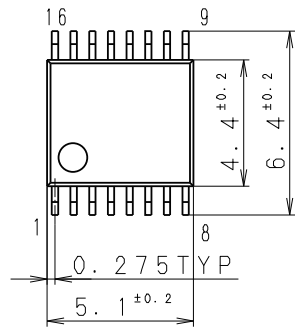
- ◆ The capacitor between CP and CN pin and connected to Vss pin are for generating negative voltage. Place these capacitors with the shortest wiring to the pins.
- ◆ The capacitor connected to Vcc pin is for smoothing noise. Place this capacitor with the shortest wiring to the pin.

Package Outline

(Unit : mm)

Product Code: 75340635/75341217

16 PIN SSOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L391
JEITA CODE	P-SSOP16-5.1X4.4-0.65
JEDEC CODE	—

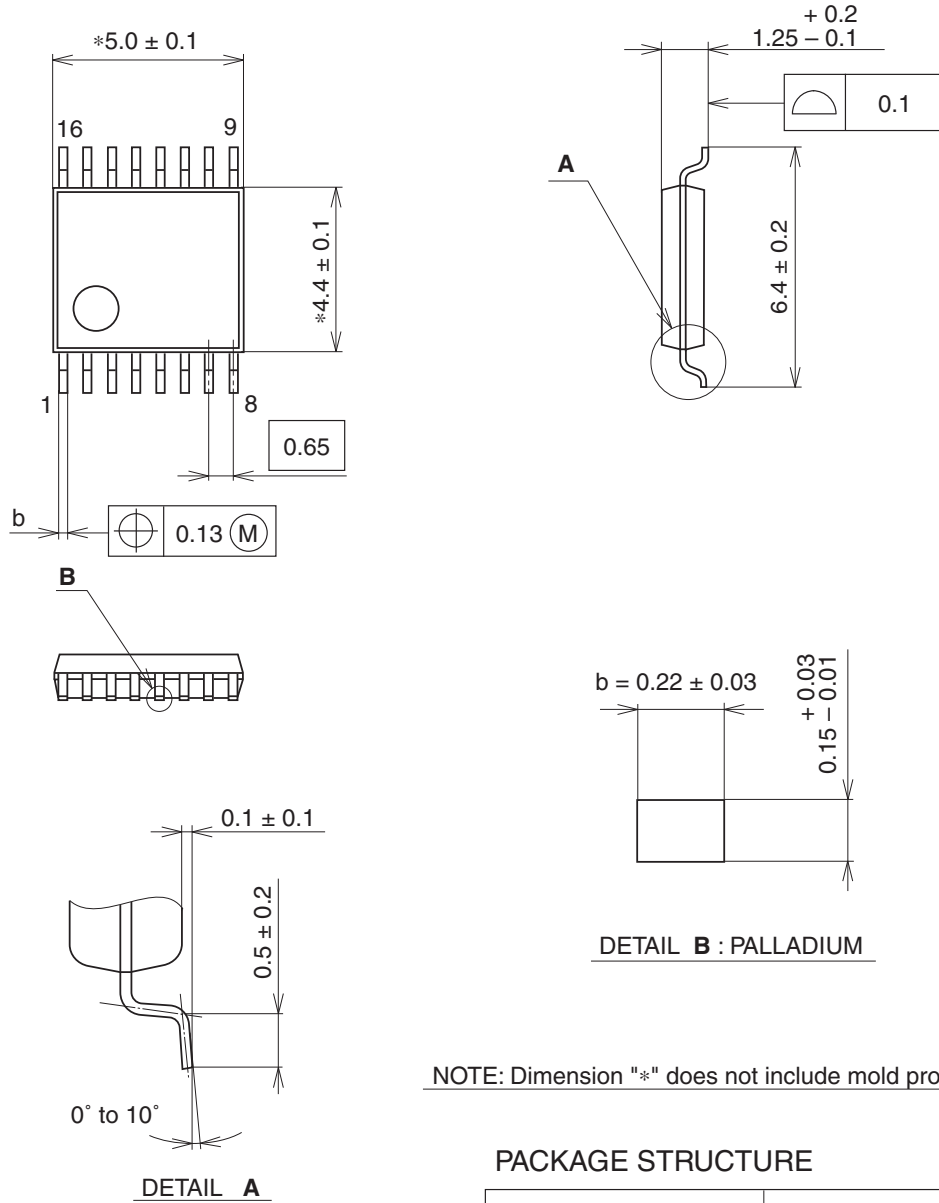
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

PART No.	AP-2000-16MAN1	Rev. 1
ISSUED	11.11.22	REVISED 11.12.28
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.	
REMARKS	PKG CODE N-16-AAN	

(Unit : mm)

Product Code: 75336351

16PIN SSOP (PLASTIC)



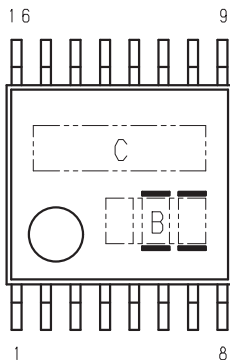
NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-16P-L01
EIAJ CODE	P-SSOP16-4.4x5.0-0.65
JEDEC CODE	_____

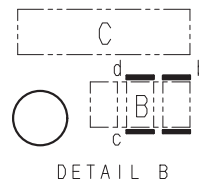
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

Marking



MARKING C: A3815

- 注1) B部はロット番号 (Max3文字で通し記号) を配置する。
 (規定文字数未満につき省略は省略規定に従う。
 製造年は下記2進法ビット方式により表示する。)
- a 部年コード (2進法ビット方式の1ビット目を表示) を配置する。
 - b 部年コード (2進法ビット方式の2ビット目を表示) を配置する。
 - c 部年コード (2進法ビット方式の3ビット目を表示) を配置する。
 - d 部年コード (2進法ビット方式の4ビット目を表示) を配置する。
- 注2) C部は製品名 (Max5文字) を配置する。
 (5文字を超える場合は製品名省略表示規定に従う。)



< INSTRUCTIONS >
 1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
 (FOLLOW RULES FOR ABBREVIATIONS.
 MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BINARY BIT SYSTEM.)
 A YEAR CODE (THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
 A YEAR CODE (THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
 A YEAR CODE (THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
 A YEAR CODE (THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
 2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
 (FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)